FIGURE 1

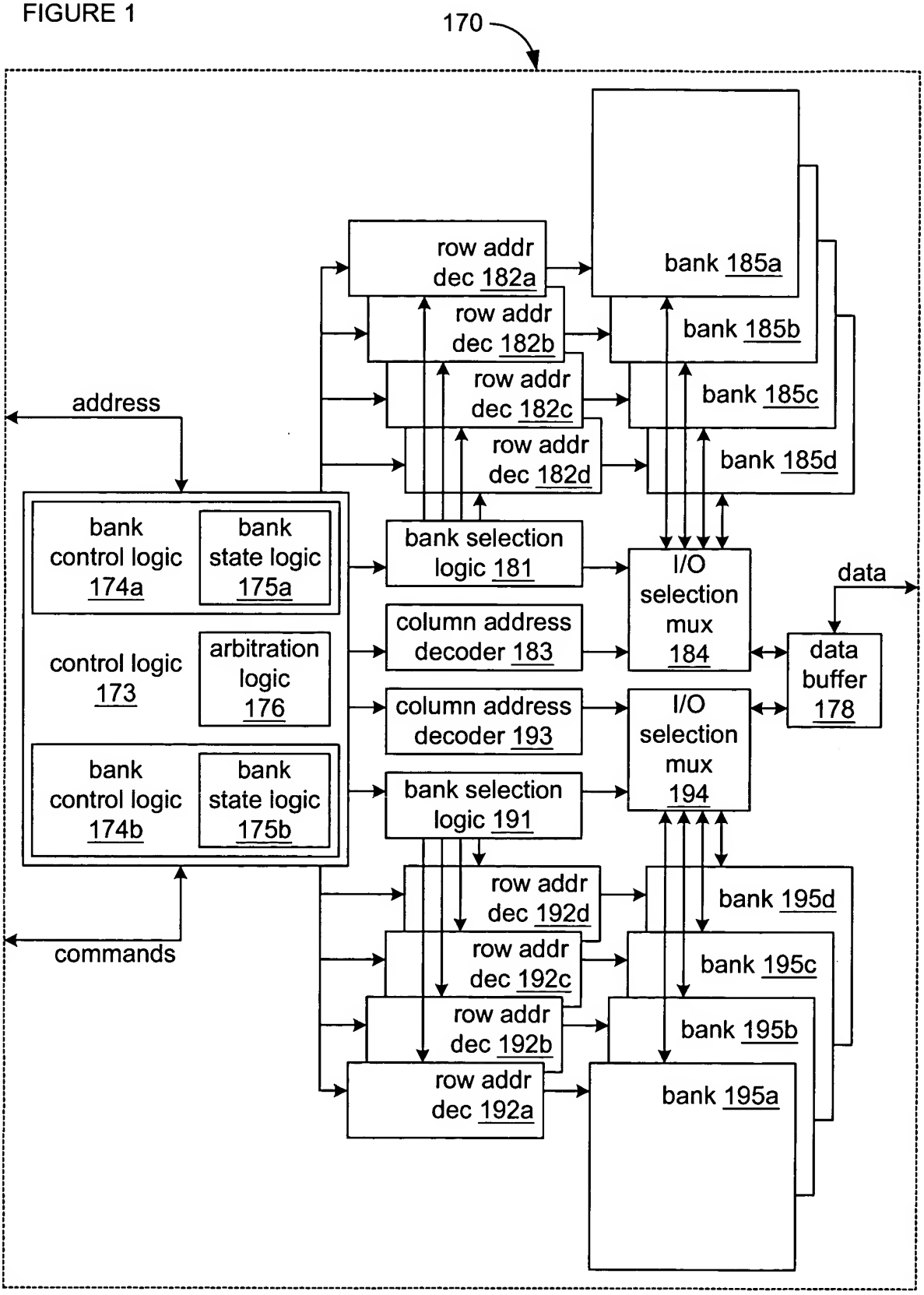
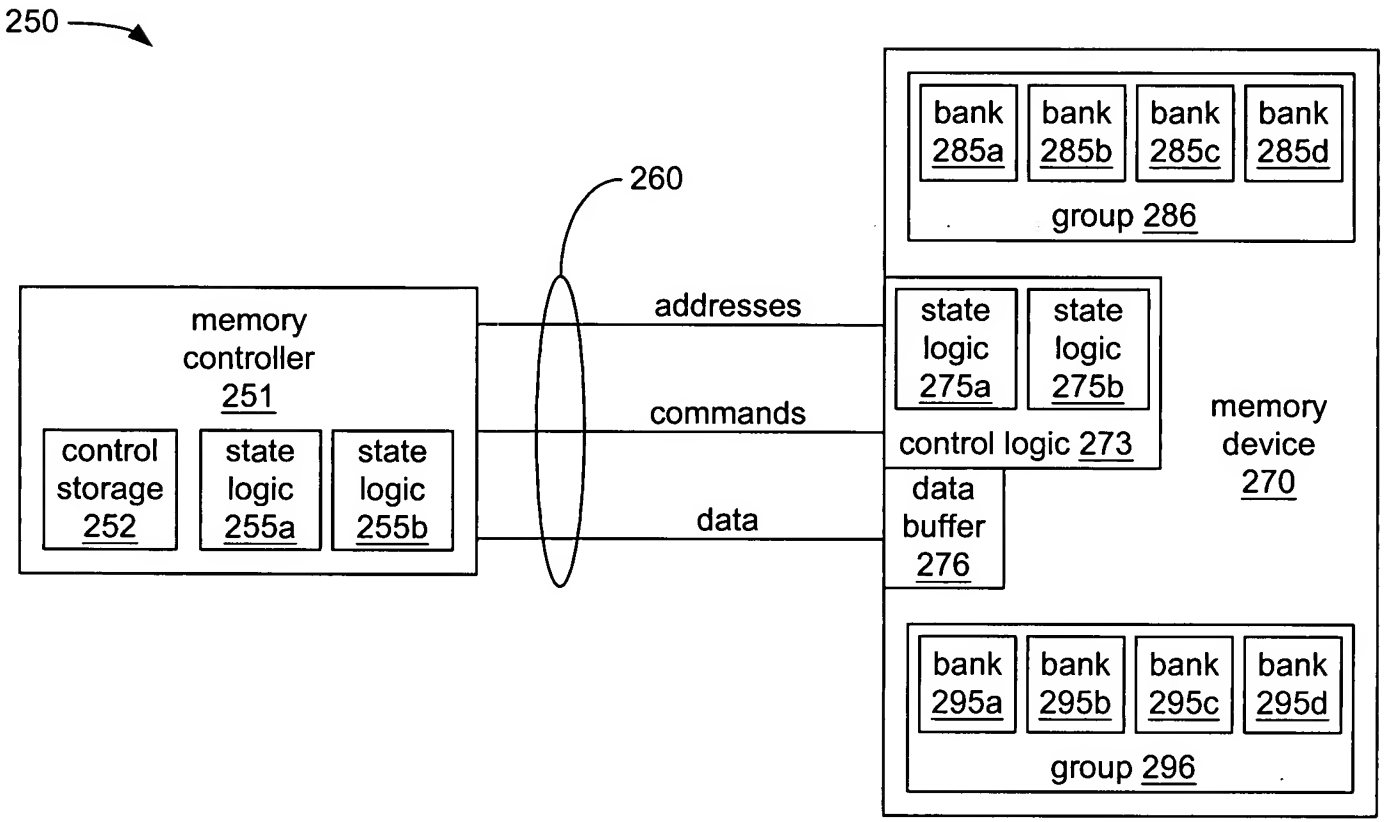

170
address
commands
bank control logic 174a
bank state logic 175a
control logic 173
arbitration logic 176
bank control logic 174b
bank state logic 175b
row addr dec 182a
row addr dec 182b
row addr dec 182c
row addr dec 182d
bank 185a
bank 185b
bank 185c
bank 185d
bank selection logic 181
column address decoder 183
column address decoder 193
bank selection logic 191
I/O selection mux 184
I/O selection mux 194
data
data buffer 178
row addr dec 192d
row addr dec 192c
row addr dec 192b
row addr dec 192a
bank 195d
bank 195c
bank 195b
bank 195a

FIGURE 2


250
260
memory controller 251
control storage 252
state logic 255a
state logic 255b
addresses
commands
data
bank 285a
bank 285b
bank 285c
bank 285d
group 286
state logic 275a
state logic 275b
control logic 273
data buffer 276
memory device 270
bank 295a
bank 295b
bank 295c
bank 295d
group 296

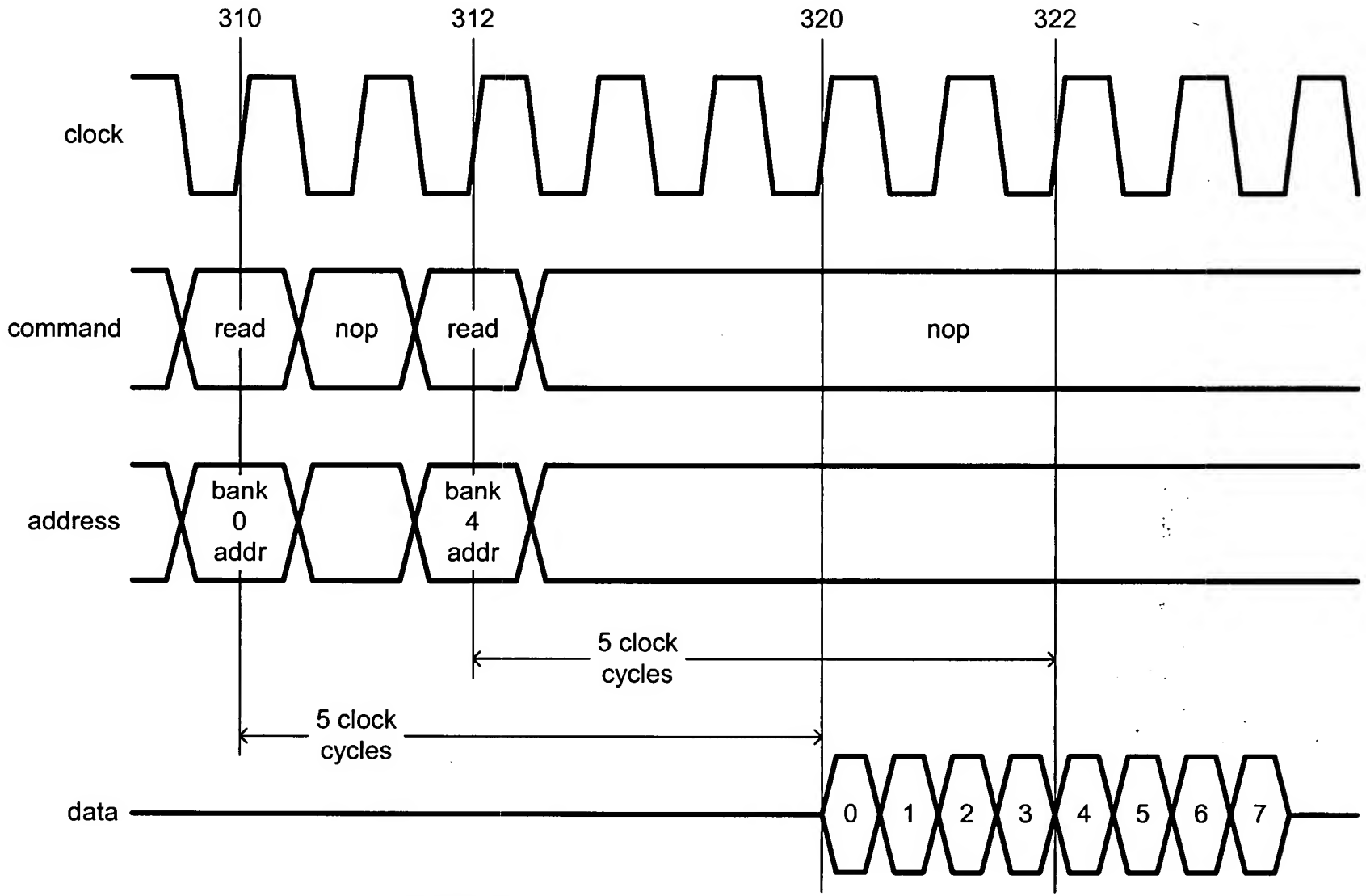

310
312
320
322
clock
command
read
nop
read
nop
address
bank
0
addr
bank
4
addr
5 clock
cycles
5 clock
cycles
data
0
1
2
3
4
5
6
7

FIGURE 3a

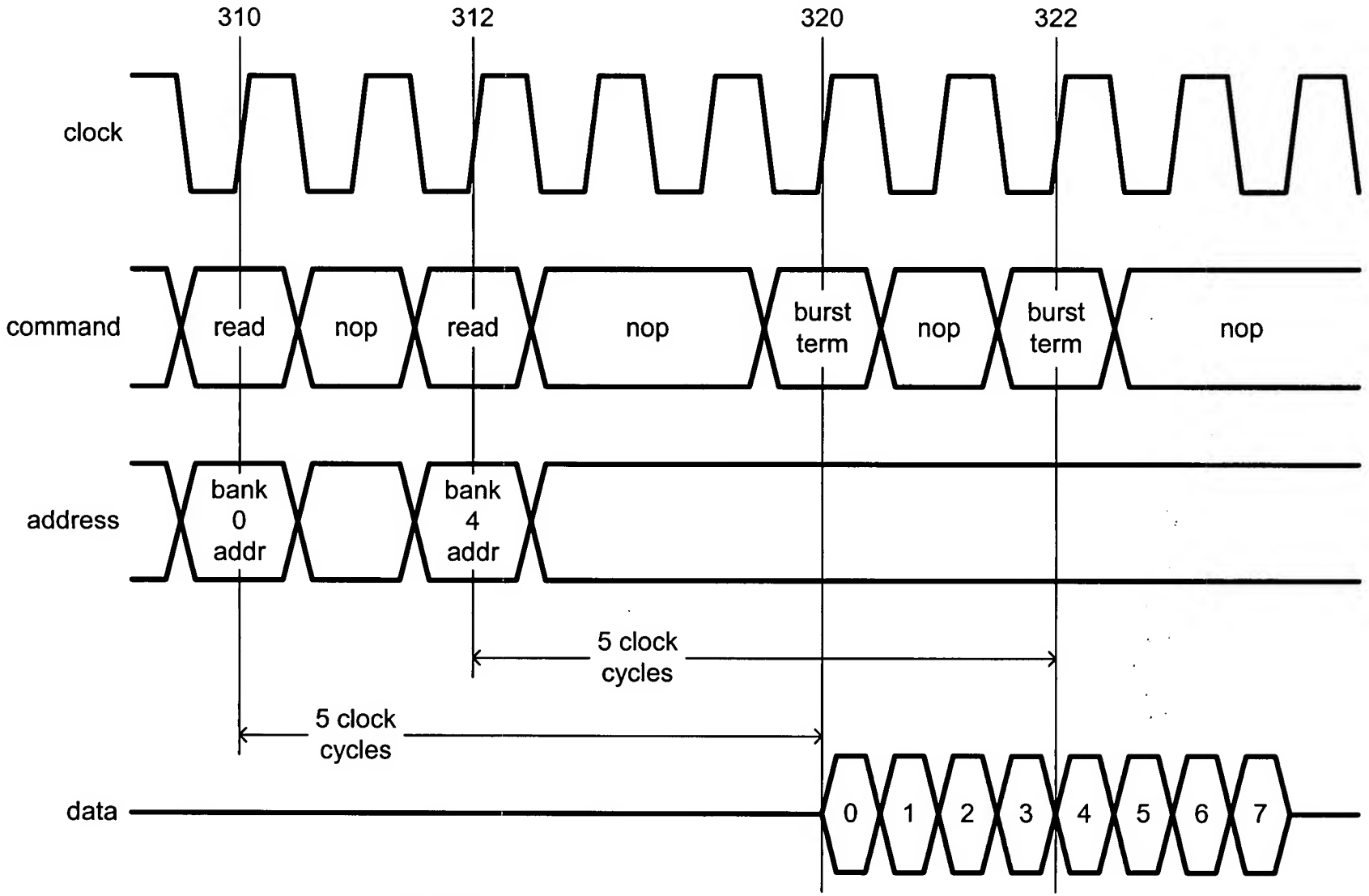

310
312
320
322
clock
command
address
data
read
nop
read
nop
burst term
nop
burst term
nop
bank 0 addr
bank 4 addr
5 clock cycles
5 clock cycles
0
1
2
3
4
5
6
7

FIGURE 3b

FIGURE 4a

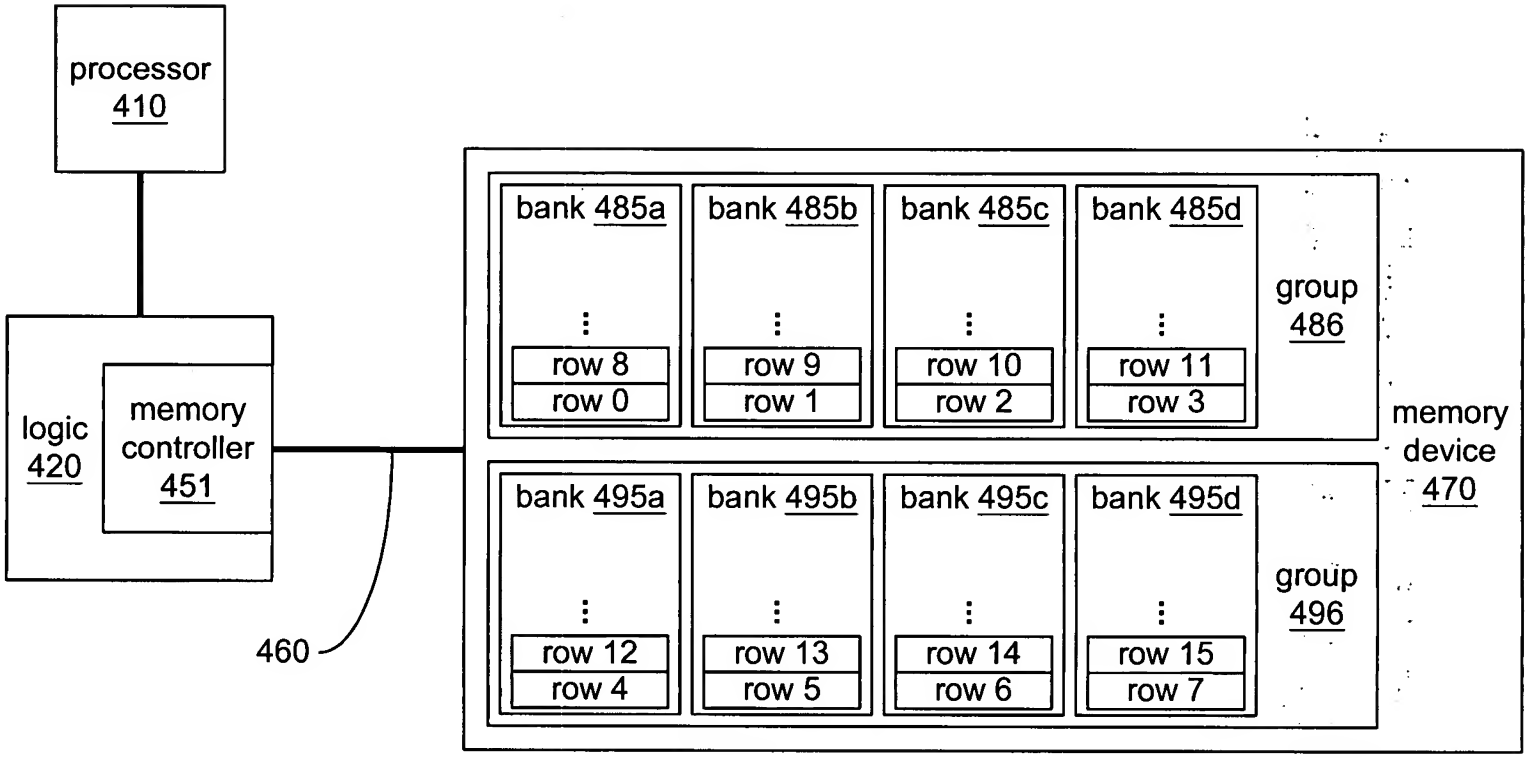

processor
410
logic
420
memory
controller
451
460
bank 485a
bank 485b
bank 485c
bank 485d
row 8
row 0
row 9
row 1
row 10
row 2
row 11
row 3
group
486
bank 495a
bank 495b
bank 495c
bank 495d
row 12
row 4
row 13
row 5
row 14
row 6
row 15
row 7
group
496
memory
device
470

FIGURE 4b

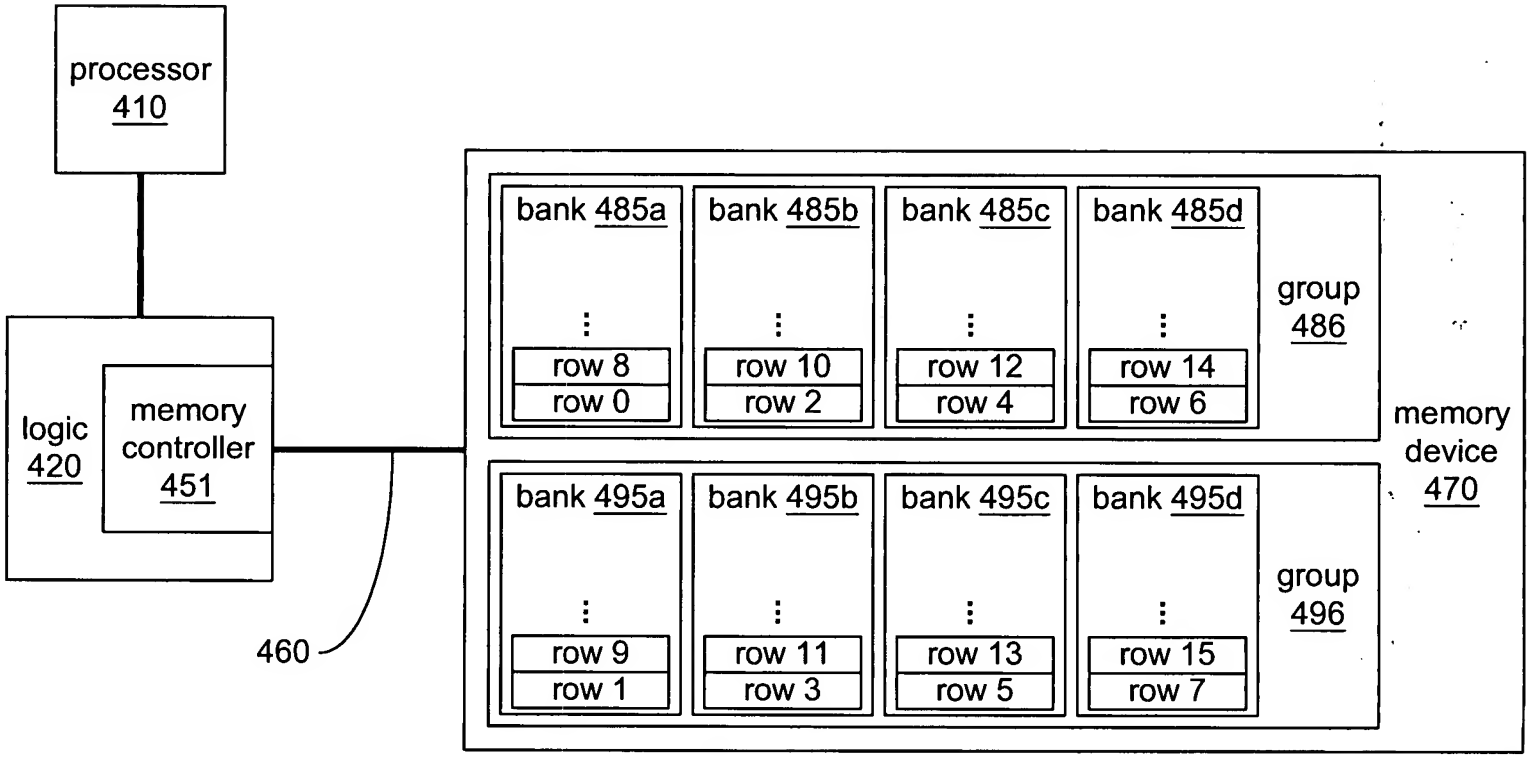
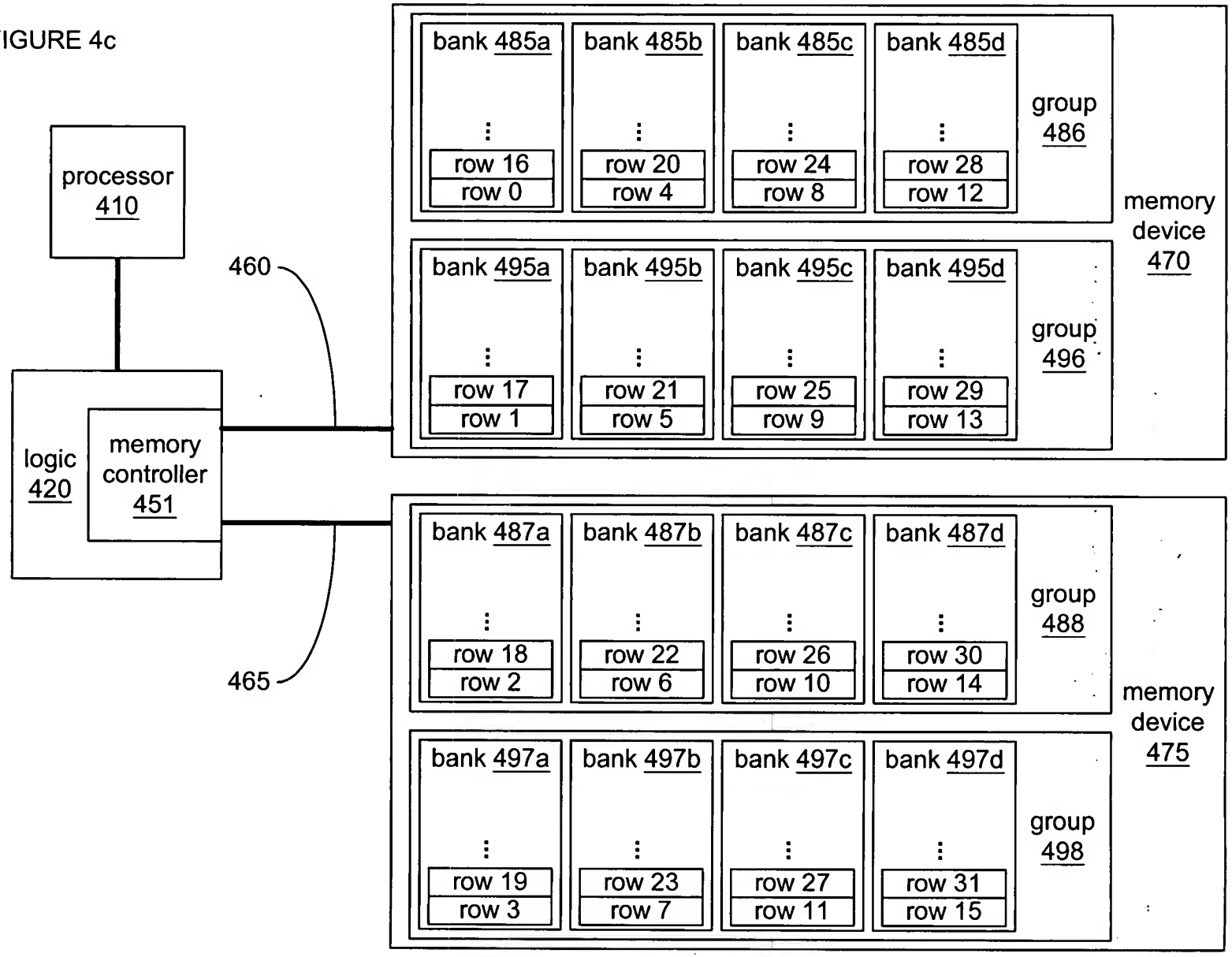

processor
410
logic
420
memory
controller
451
460
bank 485a
bank 485b
bank 485c
bank 485d
row 8
row 0
row 10
row 2
row 12
row 4
row 14
row 6
group
486
bank 495a
bank 495b
bank 495c
bank 495d
row 9
row 1
row 11
row 3
row 13
row 5
row 15
row 7
group
496
memory
device
470

FIGURE 4c


processor
410
logic
420
memory
controller
451
460
465
bank 485a
bank 485b
bank 485c
bank 485d
row 16
row 0
row 20
row 4
row 24
row 8
row 28
row 12
group
486
bank 495a
bank 495b
bank 495c
bank 495d
row 17
row 1
row 21
row 5
row 25
row 9
row 29
row 13
group
496
memory
device
470
bank 487a
bank 487b
bank 487c
bank 487d
row 18
row 2
row 22
row 6
row 26
row 10
row 30
row 14
group
488
bank 497a
bank 497b
bank 497c
bank 497d
row 19
row 3
row 23
row 7
row 27
row 11
row 31
row 15
group
498
memory
device
475

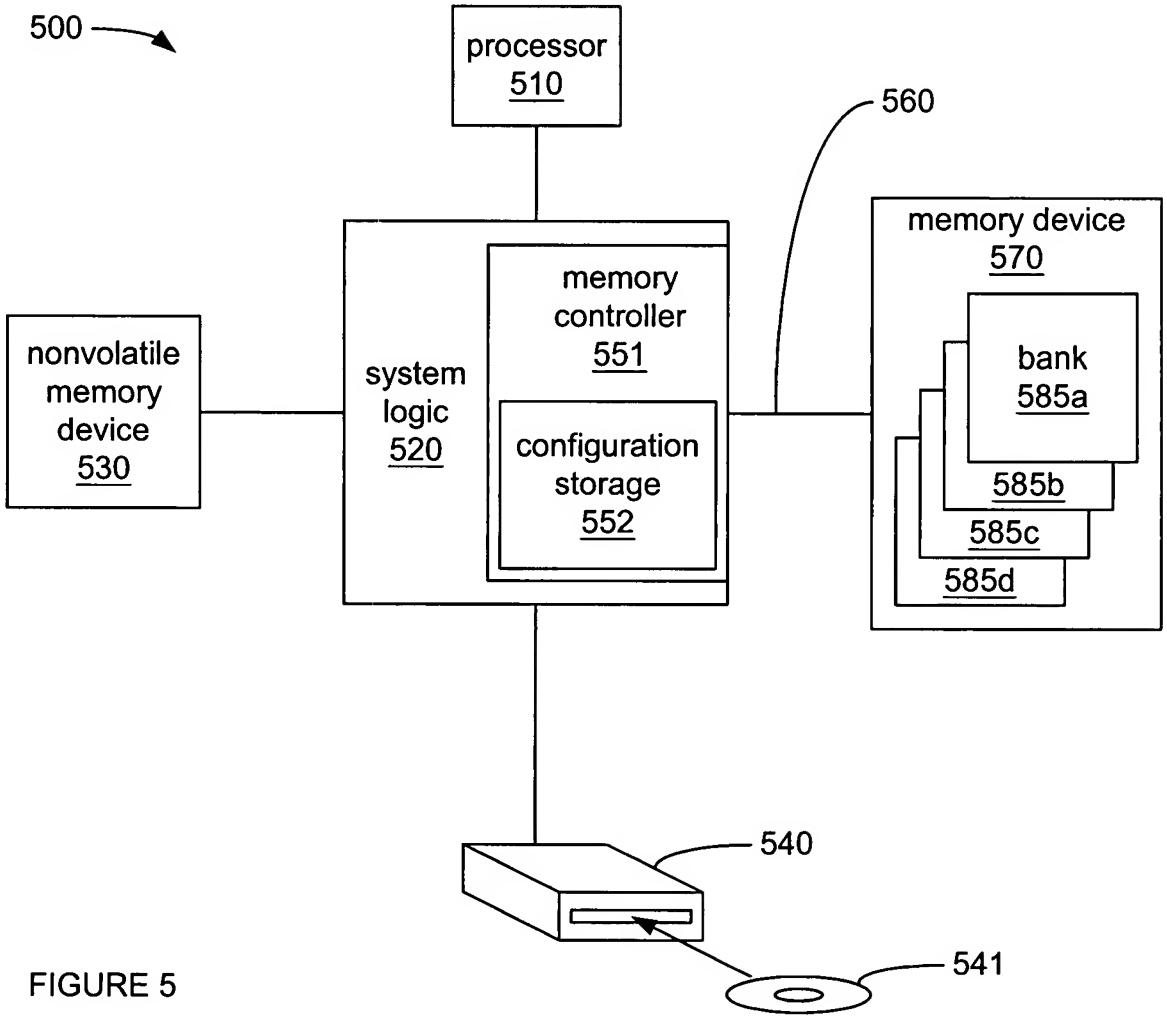
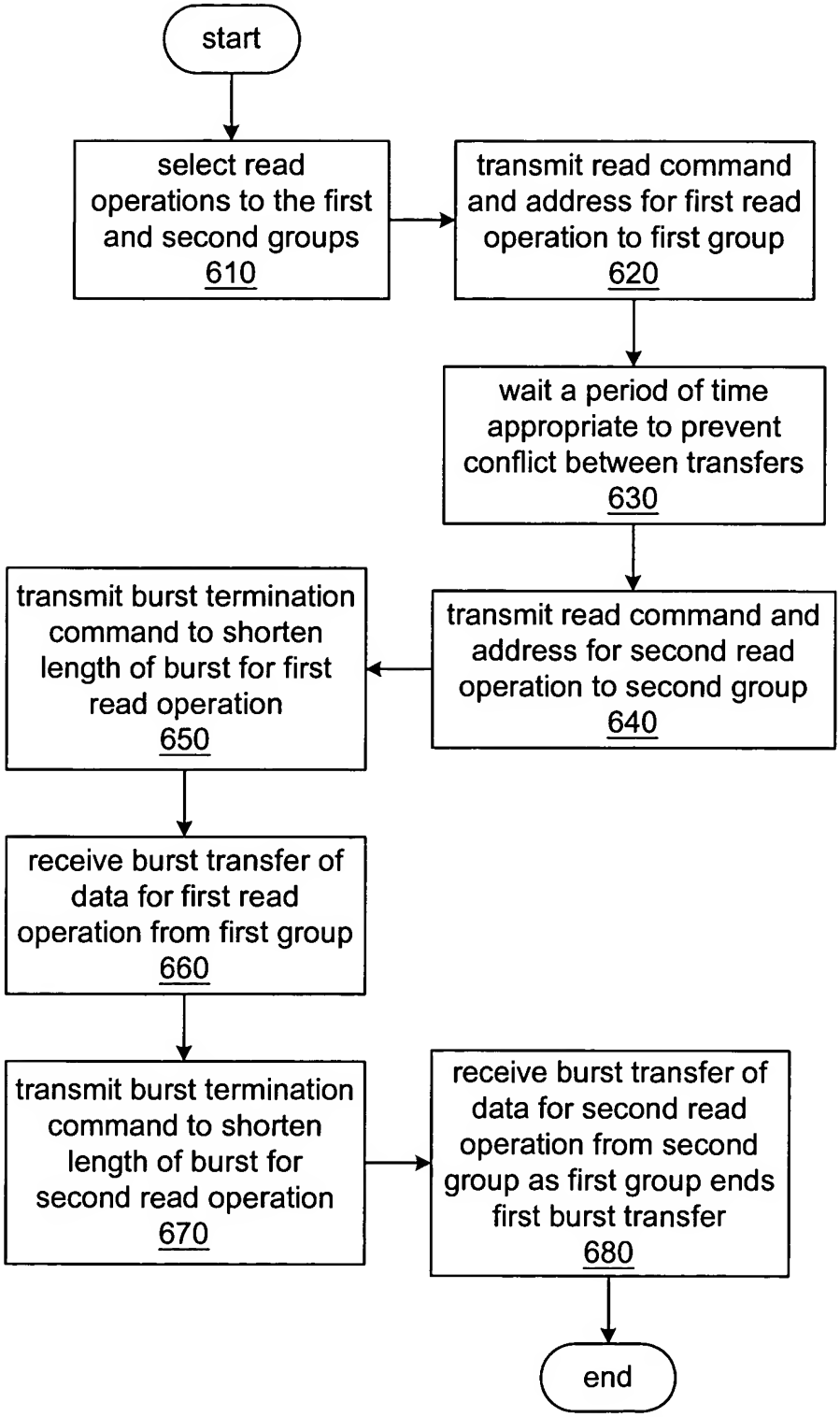

500
processor
510
560
memory device
570
memory
controller
551
bank
585a
nonvolatile
memory
device
530
system
logic
520
configuration
storage
552
585b
585c
585d
540
541

FIGURE 5

FIGURE 6


start
select read operations to the first and second groups 610
transmit read command and address for first read operation to first group 620
wait a period of time appropriate to prevent conflict between transfers 630
transmit read command and address for second read operation to second group 640
transmit burst termination command to shorten length of burst for first read operation 650
receive burst transfer of data for first read operation from first group 660
transmit burst termination command to shorten length of burst for second read operation 670
receive burst transfer of data for second read operation from second group as first group ends first burst transfer 680
end